Section IV T -Technical Specification

CENTRAL POWER RESEARCH INSTITUTE, BENGALURU/BHOPAL Web: www.cpri.in

Tender Enquiry No : CPRIBLR22HPL08C926

Description of the Equipment/Goods/Services :48-channel Test Sequencer (TS) for augmentation of short circuit test facilities at High power laboratory, CPRI Bengaluru.

Note : 1) The technical bid submitted in other than this format is liable to be rejected.

2) All blue fields are mandatorily to be filled in.

Name and address of the bidder	
Quotation Number and Date	

Sl.No.	Parameters	CPRI Technical Specification / Requirements	Qty	To be completed by the Bidder		
				Detials of guaranteed technical parameters offered by the bidder	Guaranteed Technical Particulars (GTP)	Deviations from GTP
1	Place where equipment /service to be supplied /provided	High Power Laboratory, CPRI, Bangalore.	Three nos. (03)			
2	Scope	The scope of supply includes each Test Sequencer (TS) with 48-channels, 48-power modules, all associated wiring/cabling, auxiliary supplies, Optical fiber armoured cables, Coaxial shielded cables, separate panels for placing TS, Dedicated computer, Portable programmable static device, Mandatory spares required, testing, relevant certificates, packing, delivery at site including all materials, unloading, handling, proper storage at site, installation and commissioning, site testing and training as per Section-IV Technical Specification.				
3	Qualifying Requirements (QR)	a) The supplier shall have supplied optical fiber based Test sequencer (TS) to atleast one of the High Power Short Circuit Testing Laboratory in the last Ten years. b) The supplier shall submit the proof for performance/supply of the end user in the Bid. c) Test Sequencer (TS) supplied as above shall be compatable for Prarallel operation of two or more short circuit generators. Documentary evidence shall be submitted by the supplier. d)Test Sequencer (TS) supplied as above shall be compatable for optical synchronization inputs from short circuit generators in addition to electrical reference inputs. Only one synchronization input is selected in TS at a time. Documentary evidence shall be submitted by the supplier.				

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CENTRAL POWER RESEARCH INSTITUTE, BENGALURU/BHOPAL Web: www.cpri.in, www.tenderwizard.com/CPRI

Sl.No.	Parameters	CPRI Technical Specification / Requirements	Qty	To be completed by the Bidder		
				Detials of guaranteed technical parameters offered by the bidder	Guaranteed Technical Particulars (GTP)	Deviations from GTP
Technical specification of 48-channel Tester Sequencer(TS) - Refer Annexure-I			Three no. of TS			
4	Foreword	Refer Clause 1.0 of Annexure-I				
5	Scope of supply	Refer Clause 2.0 of Annexure-I				
6	Climatic conditions	Refer Clause 3.0 of Annexure-I				
7	Reference standards	Refer Clause 4.0 of Annexure-I				
8	Functional description of HPL automation system	Refer Clause 5.0 of Annexure-I				
9	Test Sequencer general specification	Refer Clause 6.0 of Annexure-I				
10	Global test management	Refer Clause 7.0 of Annexure-I				
11	Tests on Test Sequencer	Refer Clause 8.0 of Annexure-I				
12	Documentation	Refer Clause 9.0 of Annexure-I				
13	Training, support services, maintenance and spares	Refer Clause 10.0 of Annexure-I				
14	Warranty	Refer Clause 11.0 of Annexure-I				
15	INTERCONNECTION DIAGRAM BETWEEN CMS-TS-DAS	Refer Clause 12.0 of Annexure-I				
16	PRELIMINARY LIST OF TEST SEQUENCER OUTPUT COMMANDS	Refer Clause 13.0 of Annexure-I				
17	Proposed model and configuration	The supplier shall submith the following information in the Bid; a) Test Sequencer architecture and Block Diagram; b) Guaranteed technical parameters, Hardware Specifications; c) Schematic diagrams;				
18	Bill of Material	The supplier shall submit the preliminary bill of material as per scope defined in this technical specification.				

PN: 1) Mere statement of "Complied" do not suffice the requirement. The details of technical parameters in proof of CPRI requirements shall be furnished along with technical write-up, catalogues, brouchers, literatures, phamplates, or any other documents shall be submitted in hard copy along with technical bid.
2) Calibration reports/certificates, factory test reports/certificates from an accreditated agencies/facilites shall be submitted wherever applicable.
3) CPRI reserves the right to conduct "predispatch inspection" prior to dispatch at the works of the supplier and the expenditure towards PDI shall be borne by CPRI. However information regarding the rediness of the equipment/machinary for the PDI shall be communicated in writing at lease 70 days in advance.

ANNEXURE – I

Technical Specification of
48-channel Tester Sequencer (TS)

TABLE OF CONTENTS

1 FOREWORD

Central Power Research Institute (in the following CPRI) intends to establish/augment the test facilities of the High Power Laboratory in Bangalore in order to meet the growing demand for high power testing by adding two 2500 MVA Short-circuit Generators (G2 and G3). These two Generators are to be configured in order to operate in parallel operation with the existing 2500 MVA Short-circuit Generator (G1) so that the overall short-circuit power available for the Laboratory shall amount to 7500 MVA.

The total available short-circuit power shall be used to increase the testing capability of the Laboratory (by running the Generators in parallel) and to improve the efficiency of testing activities making use the Generators individually to supply tests carried out simultaneously in different Test Facilities.

Augmentations of Test Facilities at High Power Laboratory, CPRI Bengaluru are:

- the upgrade of the Synthetic Test Facility in order to perform tests on Circuit Breakers up to 1200 kV, 80 kA;
- the upgrade of the Transformer Short-circuit Test Facility with the objective to test Transformers up to 315 MVA and 400 kV / 765 kV class;

Within the framework of this work, the implementation of a new Test Sequencer system is requested in order to cope with the new requirements determined by the envisaged new High Power Laboratory configuration.

2 SCOPE OF SUPPLY

The scope of supply includes each Test Sequencer (TS) with 48-channels, 48-power modules, all associated wiring/cabling, auxiliary supplies, Optical fiber armoured cables, Single core coaxial shielded cables, separate panels for placing TS, Dedicated computer, Portable programmable static device, Mandatory spares required, testing, relevant certificates, packing, delivery at site including all materials, unloading, handling, proper storage at site, installation and commissioning, site testing and training.

This technical Specification applies to all the Test Sequencers foreseen in High Power Laboratory (HPL), CPRI Bengaluru.

Each Control Room of HPL and STF will have its own Test Sequencer (TS), that accomplishes the purpose to perform all the commands to the objects that have to operate during Test Sequence managed from the Control Room and triggers the relevant Data Acquisition system (DAS).

The Test Sequencers mainly consist of but not limited to:

a) a software interface for the operator, typically a windows based interface running on a Personal Computer. By means of this interface the operator can build the Test Sequence, launch the Test Sequence and exchange diagnostic information with the TS hardware;
b) a suitable dedicated hardware and run-time software/firmware that are able to perform the prepared Test Sequence;
c) low power interface for the output command channels.
d) separate optically insulated output channels that operate during the Test Sequence;

e) relay modules/Power modules with normally open contacts and Type of Power module is static device based
f) separate optically insulated input channel for the voltage reference signal and pilot signal
g) Co-axial insulated input channel for the proximity sensor based pilot signal
h) Power supply for pilot signal
i) Interface from Test Sequencer output channels to controlled equipment
j) Complete hardware security against electrical/electronics interference (EMI & EMC).

The scope of supply consists of the following but not limited to:

a) 48 channels Test Sequencer with Optically insulated digital output
b) Optically insulated digital outputs of 48 channels Test Sequencer shall be connected to 48 nos. of Power modules/plant equipment with normally open contacts
c) A dedicated Software for Test Sequencer application
d) A dedicated hardware and software selection in Test Sequencer for selecting synchronising inputs i.e. pilot signals.
e) A dedicated Rack mount system for Test Sequencer, modules and accessories
f) Standalone dedicated Personal Computer (PC with latest Windows OS) suitable for operation of individual TS
g) Portable programmable static device with 8GB - RAM, 1TB – ROM, latest windows operating system
h) Suitable cable connectors for connecting to TS Power modules
i) Single core optical fiber armoured cables from pilot signal generator (Optical encoder) to Test Sequencer input for synchronisation.
j) Signal converters from (0 to 110±20)V AC voltage reference signal to optical output.
k) Single core optical fiber armoured cables from this converter to Test Sequencer input for synchronisation.
l) Single core armoured cables from pilot signal generator (Proximity sensor output) to Test Sequencer input for synchronisation.
m) Single core optical fiber armoured cables from Test Sequencer to power module input for synchronisation.
n) Single core shielded Cable for connecting relay module/Power module outputs of Test sequencer to individual equipment (ex. MCB, MS, Test Circuit Breaker, Generator Excitation, Test Start, End test commands, other equipment).
o) Each power module/channel is equipped with a status output to give feedback to the core sequencer for safety purpose.
p) The start of TS by means of hardware and software command
q) Un-interrupted Power Supply (UPS) for operation of individual Test Sequencer in case of power supply failure
r) Potential free contacts (±30VAC/DC) for each channel outputs
s) Provision for extending the number of channels upto 96 for future requirements

Before submitting the Offer, the Bidder shall visit the site (High Power Laboratory, CPRI Bengaluru) for better understanding the requirements mentioned in this technical specification with prior appointment from High Power Laboratory, CPRI Bengaluru.

The above scope is defined in general but not limited to, if anything required for successful operation of Test Sequencer is in the scope of Supplier. In the following sub sections are identified the main features of the Test Sequencer.

3 CLIMATIC CONDITIONS

The 48-channel Test sequencer (TS) and its accessories shall be designed for satisfactory operation under tropical climatic conditions prevailing in India.
The climatic conditions prevalent at the site of the operation are as follows;

a) Altitude above Mean Sea Level : 921m
b) Maximum ambient temperature : 45°C
c) Minimum ambient temperature : 10°C
d) Average annual temperature : 24°C
e) Average Humidity : 81%
f) Special corrosion conditions : Nil
g) Solar Radiation (DNI) : 4.5-5.0 kWh/Sq. m/Day
h) Atmospheric UV radiation : High
i) Pollution level : Moderate
j) Snow fall : NIL
k) Seismic Zone : Zone-II
l) Wind Speed : Average 5.6 km/h

The site location is situated in the CPRI campus located adjacent to Indian Institute of Science. The site can be approached

a) By Train: Nearest Railway station: Yeshwanthpur
b) By Air: Kempegowda International airport 33 km away from site.
c) Nearest Sea Port: Chennai

4 REFERENCE STANDARDS

This Technical Specification define the conditions that Test Sequencer (TS) and their accessories must satisfy, as regards the design, manufacture, characteristics, ratings and qualification testing to be implemented in order to establish their compliance with the requirements of this Technical Specification.

The Test sequencer and their accessories shall comply the following reference IEC Standard:

Electrical Safety

- IEC 61010-1 Safety requirements for electrical equipment for measurement, control, and laboratory use - General requirements,
- IEC 61010-2-030 Particular requirements for testing and measuring circuits.

Electromagnetic Compatibility

- IEC 61326-1 Electrical equipment for measurement, control and laboratory use EMC requirements - Part 1: General requirements

Emission

- IEC 61000-3-2 Limits for harmonic current emissions,
- IEC 61000-3-3 Limitation of voltage changes, voltage fluctuations and flicker in public low voltage supply systems.

Immunity

- IEC 61000-4-2 Electrostatic discharge immunity test (ESD);
- IEC 61000-4-3 Radiated, radio-frequency, electromagnetic field immunity test;
- IEC 61000-4-4 Electrical fast transient/burst immunity test;
- IEC 61000-4-5 Surge immunity test;
- IEC 61000-4-6 Immunity to conducted disturbances, induced by radio-frequency fields;
- IEC 61000-4-11 Voltage dips, short interruptions and voltage variations immunity tests;

In the matter of conformity, the following order shall be binding:

- The requirements of this specification,
- The latest versions of IEC Publication,
- To the latest versions of other national/international standards/codes as applicable to the relevant equipment or component or the material used in the manufacture of the same.

In the event a requirement is not covered by any of the above mentioned documents the same shall be decided by mutual agreement between the Supplier and CPRI.

5 FUNCTIONAL DESCRIPTION OF HPL AUTOMATION SYSTEM

The overall HPL Laboratory management system, that manages the set-up and execution of tests in HPL Test Facilities, consists mainly in three parts:

- Control and Monitoring System (CMS);
- Data Acquisition System (DAS);
- Synchronisation system needed to operate the different equipment (laboratory equipment and equipment under test) during the tests: Test Sequencer (TS).

The Control and Monitoring System (CMS) performs several tasks:

- Access Control and Safety: the CMS watches over safety of people working in the Laboratory and over access in the various Laboratory areas, for example to perform circuit connections and maintenance on the installed equipment ;
- Test Circuit Configuration: the CMS configures the test circuit (at least partially, being some of the operations carried out manually);
- Test Process Control: the CMS, operating together with the dedicated Control Systems of the HPL power sources (short circuit generators, DC voltage generators of the Synthetic Test Facility, etc.), prepares the selected power sources for the test, monitors the status of tests circuit equipment and of some of the test parameters (voltage and current) and interacts with the DAS and TS;
- Protection: the CMS controls HPL protection relays and related alarms.

When the test circuit is ready to provide power to object under test, then the CMS enables the Test Sequencer to perform the defined Test Sequence (the Test Sequence is a sequence of commands required for the performance of the test, intentionally started by the operator, and carried out automatically according to a pre-established timing, independently from the operator control).

The Test Sequencer shall perform the test sequence and shall have to trigger the Data Acquisition System (DAS) which acquires the defined quantities (current, voltage, etc.) for the test duration and

shall work in hand shaking mode with CMS during parallel operation, which foresees the TS to operate for longer duration as mentioned in clause 6.0 of this specification.

At the end of the test, the Test Sequencer releases the control of the plant that is resumed by the CMS. **Figure 1** shows a simplified interconnection diagram of the above mentioned systems. A more detailed interconnection diagram is in the clause 11.0 of this document.

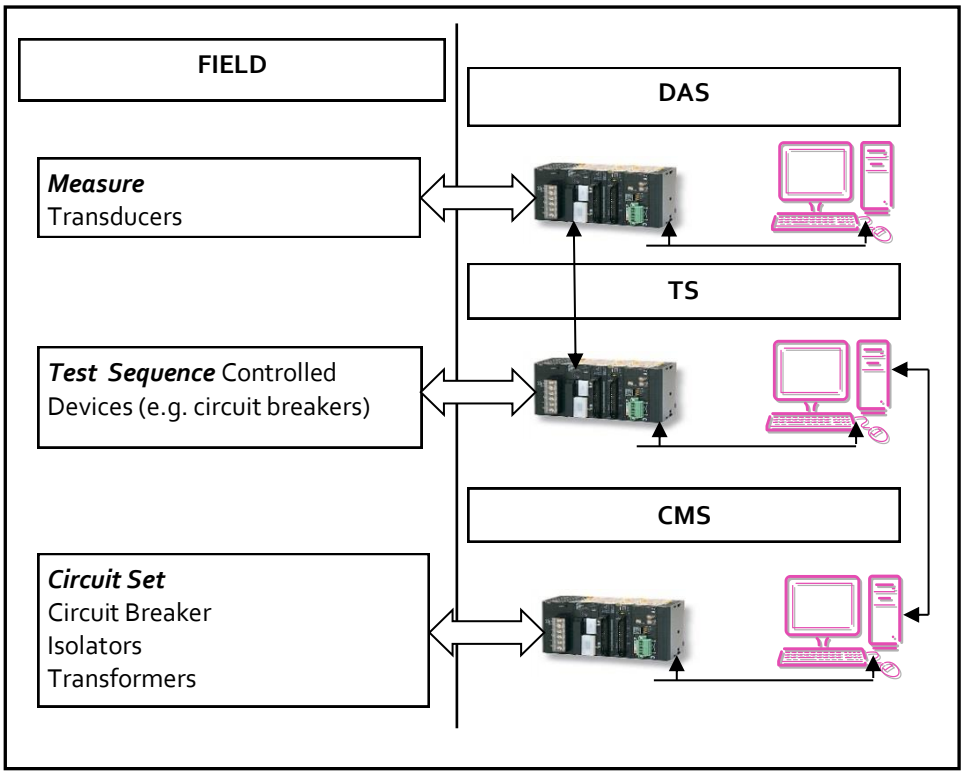


Figure 1 – Systems involved in the management of testing activities

One CMS shall manage all the Testing Facilities, each Test Facility shall be provided with its own TS and DAS.

The present document provides the Test Sequencer specifications, while the Automation and Control system (CMS) and the Data Acquisition System (DAS) will not be in the scope of supplier.

Test Execution

Briefly the test execution is a process which involves the Three Systems.

Before starting test the operator has to perform:

- set of the test circuit with CMS;
- set the TS, preparing the correct sequence of commands to be executed;
- set data acquisition system and display system (DAS), preparing input ranges (full scale) table, parameters to display output data and sampling rate (out of the scope of this document).

When all these activities are achieved and all the equipment are ready to start, the operator can start the Test Sequence.

At the end of the Test Sequence:

- The CMS resumes the control of the laboratory configuration,
- The TS is disabled,
- The DAS processes the acquired data and display the test results.

6 TEST SEQUENCER GENERAL SPECIFICATION

Test Sequencer Input	
Reference Signal for synchronization process	Pilot Signal(s) selection 1. Sinusoidal Signal Electrical input : 110Vrms 50/60Hz from VT output 2. Short circuit Generator digital signals (Optical input from optical encoder from the Generator rotor shaft) 3. Proximity sensors output pulses with±24Vpeak #
Maximum frequency variation of voltage reference signal	± 20% at 50Hz, 60Hz & 66Hz
Maximum variation of voltage reference signal	0-110%
Test Sequencer Output	
Number of channels	48
Type of outputs	Normally open contacts (10A a.c/d.c. up to 230Va.c/d.c.) made with Power Module
Resolution	≤ 1 electrical degree at 50 Hz and 60Hz
Accuracy	≤ 0.5 electrical degree at 50 Hz and 60Hz ±0.05%
Test Sequencer Internal Interface	
Interface between Main hardware and Power output	Optically isolated
Test Sequencer Software	
Number of commands during the Test Sequence	not less than 200
Test sequence duration	not less than 3600 sec
Test sequence configuration	Test sequencer software shall be Graphical User Interface type and it allows the operator to prepare and adjust the test sequence options.
Test sequencer few features	a) Each power module/channel is equipped with a status output to give feedback to the core sequencer for safety purpose. b) A dedicated hardware and software

	selection in Test Sequencer for selecting synchronising inputs i.e. pilot signals.
Power Supply Requirement	
Rated Supply Voltage	230 Vac (± 10%)
Rated Supply Frequency	50 Hz (± 5%)
Un-interrupted Power Supply (UPS) rating required for continuous operation	Suitable rating to be specified and supplied by the supplier for a backup duration of not less than one hour.

Rectangular or triangular signal from proximity sensors placed near teethed wheel of the short circuit generator rotor shaft. The output of proximity sensors is neither triangular nor rectangular; the signals shall have DC bias. These signals shall be converted to a pulsed signal by means of a suitable processing circuit of the test sequencer as per the test sequencer requirement.

The Test Sequencer shall have a dedicated hardware mainly divided in two parts:

a) A dedicated section which is able to perform a Test Sequence of timed action within a specified time interval (cycle duration). This controller shall have a suitable internal time base in order to achieve each delay between subsequent timed actions, this internal time base shall comply with the delay time resolution, therefore shall not be greater than 50 µs. Internal time base shall be also available as output in TTL form through BNC connector for recording purpose.

b) A dedicated section which is able to acquire a reference voltage signal from the PT/pilot signals from the proximity sensors/optical encoder placed on the rotor shaft of short circuit generator and, in run time mode, is able to detect from the reference voltage the zero crossing, the slope polarity and to compute the corresponding duration of the electrical degree (for example if frequency is 50Hz the electrical degree is about 55 µs). This information shall be used when required to synchronize some events in the test sequence to ensure a point-on-wave control respect to the reference voltage. Image of the reference voltage wave and digital TTL output of the reference voltage wave shall be available for recording purpose through BNC connector.

The sequencer systems shall be built in industrial grade cabinet confirming to international standards/practices. The Test Sequencer hardware shall have a suitable memory to store and execute the test sequence built-up as described in the next sub sections. Moreover, the Test Sequencer shall be connected to a computer network where a dedicated software will aid the operator to prepare test sequence, send this sequence to the Test Sequencer and get information from the Test Sequencer for diagnostic purpose. For example Test Sequencer could have a LAN connection port.

The sequencer shall be provided with outputs to control annunciation lamps on annunciation section to indicate the status of main power, operating mode, current status of execution, the status of power modules, boot status, healthiness of synchronising input signals. The synchronising inputs shall be optically isolated (for not less than 2.5kV) and fed to command sequencer.

The start of the Test Sequence is triggered by the operator by means of a "push button" either locally on the test sequencer or remotely (hardware or software) in the Test Sequence HMI under the following condition:

a) Test sequenced parameters are loaded in TS memory,

b) CMS has issued the information that the circuit is ready to test

The Test Sequencer shall have an internal Watch dog that control the test execution, in case of malfunction test sequence will be aborted.

One channel of the Test Sequencer shall be dedicated to safety, it will go high (output closed) during cycle execution and return low (output open) at the end of the cycle. This channel will be connected to the master breaker that shall be opened at the end of the test cycle or in case of Watch Dog alarm through the power modules with the acknowledgement to CMS.

The Test Sequencer shall have the possibility to select the source of the start trigger:

a) external hardwired trigger,
b) software trigger in the Test Sequence HMI resident on an external computer,
c) from CMS
d) Locally on the Test sequencer

6.1 Output channels

The Test Sequencer shall have 48 numbers of digital outputs that will be activated during Test Sequence.
The Test Sequencer digital outputs shall be connected via dedicated optical link to the output stage. In the output stage each command is driven by a dedicated solid state device, acting as a normally open contact. This contact will be connected to the power device which performs the open/close command of the object that has to operate during tests. The Test Sequencer output will be low power normally open contact (10 A at 230Va.c/d.c.). In case the Test Sequencer watch-dog is activated all output channel will be opened. Each output shall have a potential free contact. These Power modules shall be placed in a suitably designed industrial grade panel racks.

Each power module/channel is equipped with a status output to give feedback to the core sequencer. The software checks for the feedback and presents messages about end of sequence successful or end of sequence unsuccessful or sequence in progress etc. In case of unexpected state or feedback, an alarm is detected and the next sequence cannot be started for safety reasons. Also for safety, the sequencer is equipped with a security loop input. If this is open, the user is informed and the sequencer cannot start a sequence.

Equipment to be operated from the Test Sequencer depend on the type of test to be carried out. The Association of the Test Sequencer output channels to controlled equipment can then be done on a test by test basis, through dedicated interface boards of the CMS (Command dispatching panels in Control Rooms). However, in order to reduce time required for test preparation, it is common practice to set an association that is suitable for most of the tests and to disable output channels of the Test Sequencer linked to equipment that are not used during a specific test sequence.

Association of Test Sequencer output channels to controlled equipment shall be done by the supplier. Examples of most demanding configurations are given in clause 12.0 of this document (intended to demonstrate that the specified number of Test Sequencer output channels is enough to cope with the foreseen test sequences). Clause 12.0 of this document is only for information purpose.

Examples of typical output commands to be provided by the Test Sequencer are the following:

Output commands	**Test Cells**
Start/stop of generators excitation	All generators used for the test
Start/stop of generators motor	All motors used for the test
Start/stop of generators super excitation	All generators used for the test
Closing/opening of generators master circuit-breakers	All generators used for the test
Closing/opening of MV making switches (pole by pole)	All generators used for the test
Closing/opening of MV/HV/EHV test breakers	Circuit Breaker Test Cells

The above sequences are only for indicative purpose, the selection of output commands will be finalised during the commissioning of the test sequence where all the 48channels will be used for the executing different sequences depending on the test.

6.2 Test sequence

Test sequence is a sequence of commands to Laboratory equipment that must operate during the test execution. The system shall be designed such that the sequence is reliably executed even in case of heavy electrical noise on the main power lines.

Work experiences in testing laboratories suggest the following approach for preparing a test sequence. Other solutions are acceptable, as long as the proposed implementation is user friendly and the required timing and degree resolution are respected. Moreover equivalent solution shall assure the specified performance.

The Test Sequence is defined by the operator by means of a Configuration software, preferably with a graphical user interface/tabular interface.

Each event that shall happen during test execution is identified by the operator and associated to a specific point of the test sequence. Each event is started through the activation of a dedicated output channel with a specified delay from the actual start of the Test Sequence.

The synchronization of the beginning of the Test Sequence is performed with the pulses taken from any one of the following;

1) From the teethed rotor by means of proximity sensors. One pulse indicating complete rotation/full cycle of sine wave and 200 pulses for each rotation/full cycle of sine wave, for point on wave control.
2) A voltage signal generated from the output of the PT connected to the generator terminals is fed to the test sequencer. The test sequencer shall have a dedicated hardware for generating the required synchronizing pulses from this reference voltage signal for point on wave control.
3) The pulses generated from the optical encoder located on the same generator(s) shaft

The test sequencer must have provision for accommodating all of the three modes described above.

The actual instant of every event is therefore known only during cycle execution (run time).

Any one of the three synchronization input defined above shall be selected for the initiation of test sequence process.

The user specific command sequence shall be first programmed in the Test Sequencer PC (Personnel Computer). This sequence shall be programmed at any desired resolution of not more than 0.1mSec

or 1 electrical degree, number of loops, delay between loops etc. These sequences shall be stored for future use.

The desired command sequence shall be selected/programmed and loaded just before actual test. The sequence is then be transmitted to the main system using the proprietary communication link and multi-way cable. The annunciation lamp indicating receiving data shall glow during transmission.

The ready to operate lamp shall glow after successful data reception from the PC. Pressing the start command (provision for both wired and soft signal shall be made) either from local or remote shall now operate the test sequence, after the ready command from the CMS. The remote trigger located on the main test control desk shall be also operate the test sequence.

A mock run shall be conducted prior to actual testing by keeping the 'Output' inactive and pressing the start switch. The sequence shall be executed as seen on annunciation panel LEDs.

The outputs of all relay modules/power modules and potential free contacts shall initially in normally Open/Close condition (as per the user requirement). On receiving the trigger all the relay modules/power modules and potential free contacts shall be coupled logically to the test sequencer, on recognizing a valid zero crossovers. The sequences, which controls the ON and OFF conditions of the outputs relay modules/power modules and potential free contacts, is already resident in the individual command sequencer. The command sequencer begins execution after preset initial delay and shall also be indicated by the test in progress annunciation lamp. The out relay modules/power modules and potential free contacts follow the binary patterns of the sequence and thus Close and Open independently. The test sequence shall be repeated if programmed so by the user.

The test sequencer shall terminate the operation on completion of test sequences and all output relay modules/power modules and potential free contacts shall return to normally Open/Close condition. The end of test sequence shall be informed to the CMS by suitable command.

The system shall automatically be switched to the internal battery source for power during execution of sequence. This ensures that the sequence shall be completed reliably even in case of mains power corruption during test execution.

The test sequence shall consists of more than 10 closes and 10 opening of output relay modules/power modules and potential free contacts set at time intervals with respect to trigger event. The user interface shall allow use of relative time intervals within a channel while setting up a test sequence.

This test sequence shall be repeated as many as hundred times in a day as programmed in number of cycles by the user. The delay between individual sequences shall be set to a maximum duration of 3600 seconds with a resolution of 1 second.

Every object operating during test cycle has its own lead time and command duration[1], these are specific of each object and they have to be taken into account for cycle execution accuracy. The Test

[1] Lead time: is the time between the command start and its completion, for example a master breaker opening time.

Sequence shall be defined so as to issue the command in advance, to assure the end of equipment operation at the correct instant. Furthermore the output channel will be active for the time needed to carry out the operation.

Once the test sequence has been defined by the operator, it shall be compiled in such a way to be loaded into the Test Sequencer hardware and executed after a start command (trigger).

6.3 Pilot signal (Reference Signal) for synchronization process

The pilot signal(s) from Short Circuit Generator is fed as input to the Test Sequencer for synchronization process. The Test Sequencer shall be designed for synchronization process with the following pilot signal(s) received from Short Circuit Generator system;

1. Sine wave
2. Digital signals from the proximity sensor
3. Optical encoder

6.3.1 Sine wave for synchronization process

The synchronization process is based upon a dedicated card which is able to acquire the pilot signal provided by the CMS. This is a sine wave typically coming from a Voltage Transducer of Short circuit generator and conditioned in order to be acquired from the dedicated card. Usually the signal is 110±10%Vrms 50/60Hz value. The transmission between TS input reference signal card and pilot acquisition card shall be via dedicated optical link. This card shall convert the sine wave in a sequence of impulses which allows the Test Sequencer to store the duration of voltage loop and its polarity. The information that TS acquires from this card are: instant of each zero crossing and signal polarity and period duration to calculate the electrical degree value in microsecond. This process is shown in Fig. 2. (example: sine wave with a frequency of 50Hz)

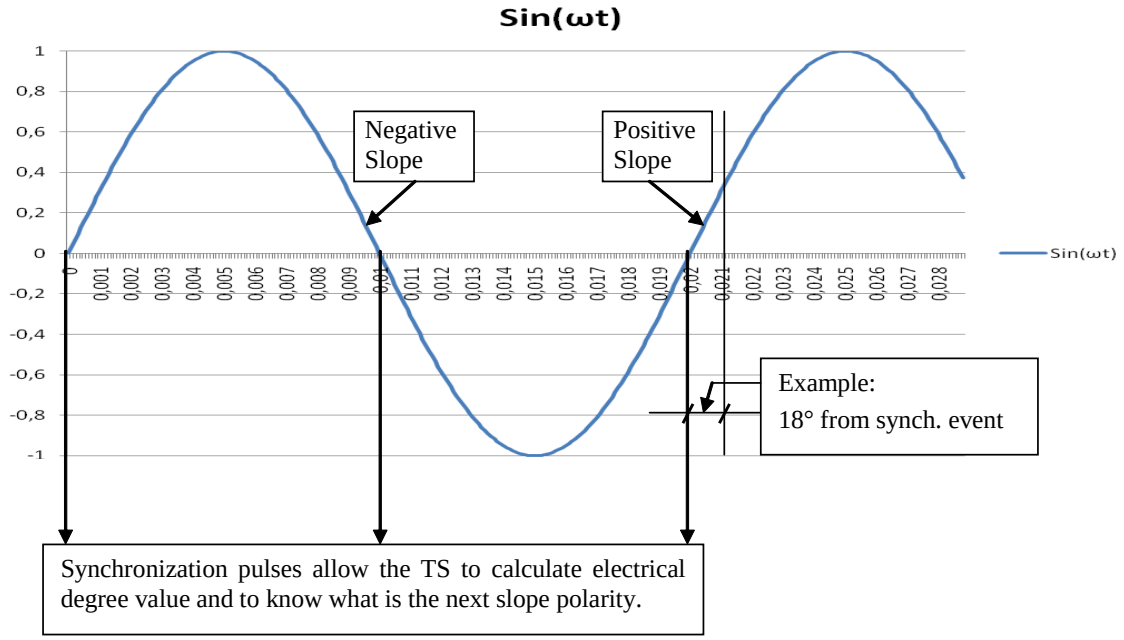


Figure 2 : Sine wave for synchronization process

Command Duration: is the minimum time that the output command have to stay active (powered) to allow the object to accomplish the operation, for example the time duration of the current in the opening coil of a circuit breaker.

6.3.2 Digital signals for synchronization process

The synchronization process is based upon dedicated cards which are able to acquire the pilot signals from Short Circuit Generator rotor shaft. They are two digital pulses typically coming from the shaft of Short circuit generator rotor and conditioned in order to be acquired from the dedicated cards. The following digital pulses are used for determine the correct angle Synchronization adjustments

a) Signal – 1: Single pulse

One pulse per rotation/sine wave from short circuit generator rotor shaft for Zero indication

b) Signal – 2: Multiple pulses

Multiple pulses per rotation/sine wave from short circuit generator rotor shaft for precise point on wave control

The single pulse and multiple pulse (200 pulses) are generated by a proximity sensors placed near the teethed wheel of the generator motor rotor line. The input voltage for the proximity sensor shall be provided by the supplier and the signal transmission to and fro from the Test Sequencer to the proximity sensors is under the scope of the supplier. These signals shall be converted to dedicated optical signal by a suitable signal converter and fed to the Test Sequencer with a minimum isolation of 2.5kV AC/DC.

Usually the signal is (+ or -) 20 to 25 V DC value. The transmission between TS input reference signal cards and pilot acquisition cards shall be via dedicated optical link, preferably optical. This card shall convert the sine wave in a sequence of impulses which allows the Test Sequencer to store the duration of voltage loop and its polarity. The information that TS acquires from this card are: instant of each zero crossing and signal polarity and period duration to calculate the electrical degree value in microsecond.

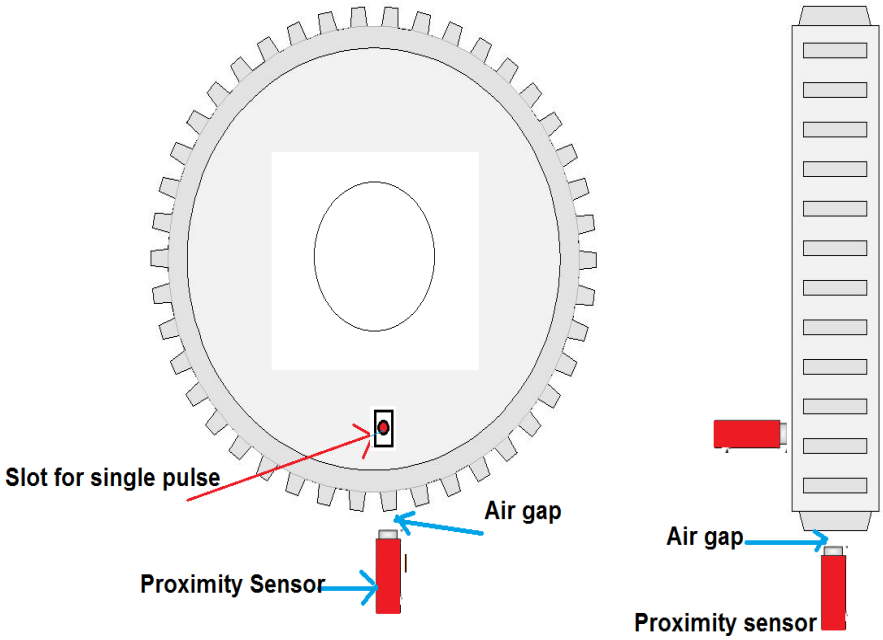


Figure 3 : Pilot signals (Single and Multiple pulse from rotor shaft) for synchronization process

6.3.3 Optical encoder signals for synchronization process

The synchronization process is based upon dedicated cards which are able to acquire the pilot signals from Short Circuit Generator rotor shaft. They are two digital pulses typically coming from the optical encoder placed on the shaft of Short circuit generator rotor and conditioned in order to be acquired from the dedicated cards. The following optical pulses are used for determining the correct angle Synchronization adjustments

a) Signal – 1: Single pulse

One pulse per rotation/sine wave from short circuit generator rotor shaft for Zero indication

b) Signal – 2: Multiple pulses

Multiple pulses per rotation/sine wave from short circuit generator rotor shaft for precise point on wave control.

6.4 Optical fiber & Co-axial shielded electrical cable

The following characteristic of optical fiber should be met:

k) Multimode Fiber 50/128 µm

l) Connector type ST made of special alloy for rough measuring environments

m) Transfer Rate 2 GB/S

Maximum cable length 200 meters but the actual length of the electrical/optical cables would be based on the actual distance between TS control room to Generator building/ various test cells. The selection of optical fiber cable shall consider the redundant for all channels.

The rating of shielded coaxial cable is based on voltage and current rating of Test sequencer Power module.

6.5 Test Sequencer Human Machine Interface (HMI)

As stated above, the Test Sequencer shall be set from a computer: the HMI software installed on this computer shall be designed to give to operator a modern, reliable an easy–to-use interface to the operator. Typically a latest Windows based interface meets these requirements.

- **Security permissions**

  Running the Test Sequencer application (for either tests sequence execution or editing) is reserved to identified members of the Laboratory staff (Test operators). The access to the SW application shall be subject to a password protected identification.

  The application can only be run by one operator at a time.

  An example of HMI is shown in fig. 4, Equivalent solutions granting the same performance are acceptable.

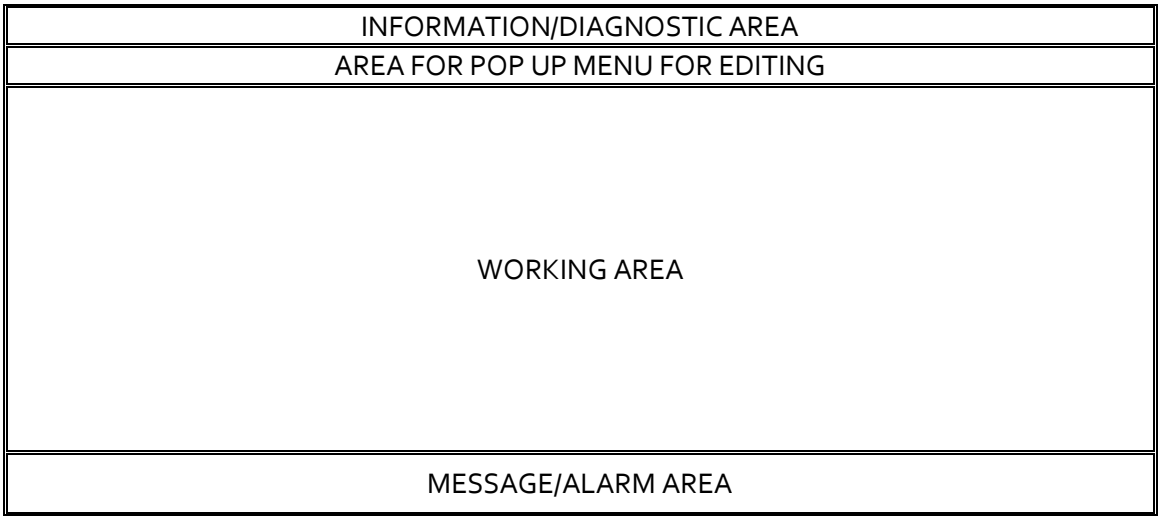


Figure 4 : Example of Test Sequencer Human Machine Interface (HMI)

The screen should be divided as follow:

- ***Information/ Diagnostic Area on the top:***

  In this area the HMI Software shall show the main information about the Test Sequencer status, the name of the Test Sequence loaded into the Test Sequencer memory, READY TO RUN, Test Sequence duration.

- ***Working Area where it is possible to set all the TS parameters:***

  In this area the operator can perform the following activities:

  A) Edit, save and recall all the set-ups related with the test sequence.
  B) Get a Graphical information about the sequence edited.
  C) Compile, Load the Test Sequence in the Test Sequencer memory.
  D) Start the Test Sequence.
  E) Get diagnostic information from the Test Sequencer.
  F) Get a Complete List of Active Test Sequencer Alarms.
  G) Get a Test Sequencer Alarms Historical List.
  H) Display the live runtime of the Test Sequence while executing the test Sequence
  I) Display the end of the test sequence after the live run time lapsed.

- ***Alarm Area at the bottom of the screen:***

  In this area the HMI Software shall show the last two incoming alarms.

When the operator has finished editing test sequence parameters and starts compilation/loading process, the software automatically shall generate a dedicated file containing the information to be given to the Test Sequencer Hardware.

It is important to note that this HMI can be a Stand-alone application or part of Data Acquisition System. In any case the software should be designed to interact with the DAS software and the operator shall have the possibility to navigate easily in both the systems.

6.6 Test Sequencer diagnostic

Front Panel Diagnostic

The front panel should have at least the following led indication:

a) Power on
b) Test Sequencer Ready to start sequence (if not lit the Test Sequencer is in alarm mode and cannot execute the sequence)
c) Sequence Aborted by operator
d) Watch Dog Alarm (eg. Feedback from power modules etc.)
e) Reference signal present
f) Synchronising pilot signals status
g) Selected trigger
h) A digital display of the time elapsed from the instant of the start of sequence to the end of sequence.
i) Synchronising signal status.

Software Diagnostic

As already mentioned above, the operator can request a diagnostic page. HMI software shall send this command to the Test Sequencer and the Test Sequencer shall reply with the information concerning hardware fault/channel diagnostic.

7 GLOBAL TEST MANAGEMENT

As already mentioned at the beginning of this document test execution involves several activities. Concerning Test Sequence and Data Acquisition, an option is that these activities can be carried out with a global dedicated software. Actions of this software are summarized below.
Preliminary operator action:

a) Prepare the Test Sequence according to the test that has to be carried out and related standard;
b) Set-up the Data Acquisition System, configuring measurement channels and data display;
c) Execute a measure channel calibration (one per daily shift).

At this point the operator can start the test. The software should act as follow:

a) Set Transmitters inputs according to the test configuration;
b) Set the Data Acquisition sampling rate as required by the operator;
c) Set the acquisition duration according to the test cycle;
d) Arm Data Acquisition Hardware;
e) Compile and Load the Test Sequence in the Test Sequencer.

At this point, if the CMS signals that the Test Circuit OK is ON (no alarm detected, circuit ready for test), the operator can push the button START TEST SEQUENCE. This will trigger the Test Sequencer and the sequence is performed, including Data Acquisition (DAS trigger comes from the Test Sequencer).

When the end of the test is reached and all the acquired data is in the DAS Hardware memory, the software will act as follow:

a) Download sampled data from DAS memory;

b) Execute all the required calculations to display the data;
c) Display the data.

When data are stored and displayed, the operator can perform data analysis on displayed data and perform all the operation of saving and recalling.

8 TESTS ON TEST SEQUENCER

The CPRI representatives shall be allowed to inspect the production process in the factory.

The Test Sequencer shall be subjected to following tests to establish compliance with the applicable Standards. The supplier shall define the test procedures to verify the performances required by the present technical specification. Such procedures shall be approved by the CPRI before the execution of the tests.

Factory Acceptance Tests performed by the manufacturer to verify the compliance of the components and/or the integrated system are not to be repeated after on-site installation.

The supplier shall submit the type test certificates of Test Sequencer including Power modules as per IEC/EN standards for the following type tests;

8.1 Type Tests (indicative list)

a) Insulation Tests:

i. Dielectric Tests;
ii. Impulse Voltage withstand Test.

b) Influencing Quantities on power supply:

i. Limits of voltage fluctuations;
ii. Permissible ripples;
iii. Interruption and dips of voltage.

c) Electromagnetic Compatibility Test:

i. 1 MHz burst disturbance test;
ii. Electrostatic Discharge Test;
iii. Radiated Electromagnetic Field Disturbance Test;
iv. Electrical Fast transient Disturbance Test;
v. Conducted Disturbances Tests induced by Radio Frequency Field;
vi. Magnetic Field Test;
vii. Emission (Radio interference level) Test;
viii. Conducted Interference Test.

d) Functional Tests:

i. Indication;
ii. Commands;
iii. Operations and sequences;
iv. Storage and retrieval;
v. Display Indications.

e) Environmental tests:

i. Cold Temperature;
ii. Dry Heat;
iii. Wet heat;
iv. Humidity (Damp heat Cycle);
v. Vibration;
vi. Bump;
vii. Shock.

8.2 Factory Acceptance Test (FAT)

The Supplier shall inform the CPRI of the Factory Acceptance Tests program 60 days in advance and shall allow the CPRI representatives to witness them.

The Supplier shall submit a test specification for factory acceptance test (FAT) and commissioning tests of the Test Sequencer for approval by the CPRI.

The general philosophy shall be to deliver a system to site only after it has been thoroughly tested and its specified performance has been verified, as far as site conditions can be simulated in a test lab. During FAT the complete Test Sequencer to be supplied under the present scope shall be tested for complete functionality and configuration in the factory itself. The purpose of Factory Acceptance Testing is to ensure trouble free installation at site. No major configuration setting of system is envisaged at site.

If the complete system consists of parts from various suppliers, the FAT shall be limited to sub-system tests. In such a case, the complete system test shall be performed on site together with the site acceptance test (SAT).

8.2.1 Hardware Integration Test

The hardware integration test shall be performed on the specified systems to be used for Factory tests when the hardware has been installed in the factory. The operation of each item shall be verified as an integral part of system. Applicable hardware diagnostics shall be used to verify that each hardware component is completely operational and assembled into a configuration capable of supporting software integration and factory testing of the system. The equipment expansion capability shall also be verified during the hardware integration tests. The supplier specifically demonstrates how to add a device in future to the Test Sequencer during FAT.

8.2.2 Integrated System Test

Integrated system tests shall verify the stability of the hardware and the software. During the tests all functions shall run concurrently and all equipment shall operate without errors and malfunctioning for a continuous period (duration of the tests shall be approved by the CPRI). The integrated system test shall ensure that the Test Sequencer is free of improper interactions between software and hardware while the system is operating as a whole.

8.3 Site Acceptance Test

The site acceptance tests (SAT) shall completely verify all the features of Test Sequencer hardware and software. The supplier shall submit the detailed SAT procedure to the CPRI for approval.

Site Acceptance Tests shall verify normal operations (start-up, sequence management, storage and retrieval of settings, back-up, shut-down, etc.) and abnormal but expected situations (for example cycle interruption, loss of data, human errors, system faults).

9 DOCUMENTATION

The following documentation to be provided for the system in the course of the project shall be consistent, CAD supported, and of similar look/feel. All CAD drawings shall be provided in "dwg" format.

a. Test Sequencer architecture and Block Diagram;
b. Guaranteed technical parameters, Hardware Specifications and Guaranteed availability and reliability;
c. Assembly drawings, schematic diagrams, List of Apparatus, List of Labels;
d. Test Specification for Factory Acceptance Test (FAT) and Site Acceptance Test (SAT);
e. Product Manuals;
f. Operator's Manual;
g. Listing of software and loadable in USB;
h. Other documents as may be required during detailed engineering.

10 TRAINING, SUPPORT SERVICES, MAINTENANCE AND SPARES

10.1 Training

The Supplier shall arrange on its own cost all hardware training platform required for successful training. The Supplier shall provide all necessary training material: each trainee shall receive individual copies of all technical manuals and all other documents used for training. These materials shall be sent to the CPRI before the scheduled commencement of the training course.

The Supplier shall quote training prices. The schedule, location, and detailed contents of the training course will be finalized during CPRI and Supplier discussions.

10.2 Test Sequencer System Hardware Course

A course focused on the Test Sequencer hardware shall be offered, to give CPRI's personnel sufficient knowledge of the overall design and operation of the system so that they can correct obvious problems, configure the hardware, perform preventive maintenance, run diagnostic programs, and communicate with Supplier's maintenance personnel. The following subjects shall be covered:

a. System Hardware Overview.
b. Configuration of the Test Sequencer hardware equipment.
c. Equipment Maintenance: Basic theory of operation, maintenance techniques and diagnostic procedures for each element of the system.
d. System Expansion: Techniques and procedures to expand and add equipment such as output modules, monitors, and communication channels.
e. Hands on Training: this training shall be provided on CPRI equipment, or on similarly configured systems.

10.3 Application Software Course

The Supplier shall provide a comprehensive course on the test Sequencer application software, covering all functions. The training shall include:

a. Overview of the application software and data flows.

b. Test Sequence setting procedures: start-up, definition of the test sequence, storage and retrieval of settings, back-up, shut-down.
c. Hands-on Training: this training shall be provided on CPRI equipment, or on similarly configured systems.

10.4 Maintenance Responsibility during the Guaranteed Period

During the Guarantee Period as specified in tender documents, the Supplier shall take continual actions to ensure the guaranteed system availability and shall make available all the necessary resources such as specialist personnel, spare parts, tools, test devices etc. for replacement or repair of all defective parts and shall have prime responsibility for keeping the system operational.

10.5 Reliability and Availability

The Test Sequencer shall be designed so that the failure of any single component, processor, or device shall not render, as far as possible, the system unavailable. The Test Sequencer shall be designed to satisfy the very high demands for reliability and availability concerning:

a. Mechanical and electrical design;
b. Security against electrical/electronics interference (EMI & EMC);
c. High quality components and boards;
d. Modular, well-tested hardware;
e. Thoroughly developed and tested modular software;
f. Easy-to-understand programming language for application programming;
g. Detailed graphical documentation and application software;
h. Built-in supervision and diagnostic functions;
i. Security;
j. Distributed solution;
k. Independent units connected to the local area network;
l. Back-up functions;
m. Panel design appropriate to the harsh electrical environment and ambient conditions;
n. Panel grounding immune against transient ground potential rise.

The availability for the complete Test Sequencer shall be guaranteed by the Supplier. The Supplier shall include in the offer the detailed calculation for the availability.

10.6 Spares & Maintenance

The supplier shall have to propose and quote for mandatory spares, which are mandatory to be procured for first five years normal operation. Mandatory spares quote shall be included in the main equipment cost for bid evaluation purpose.

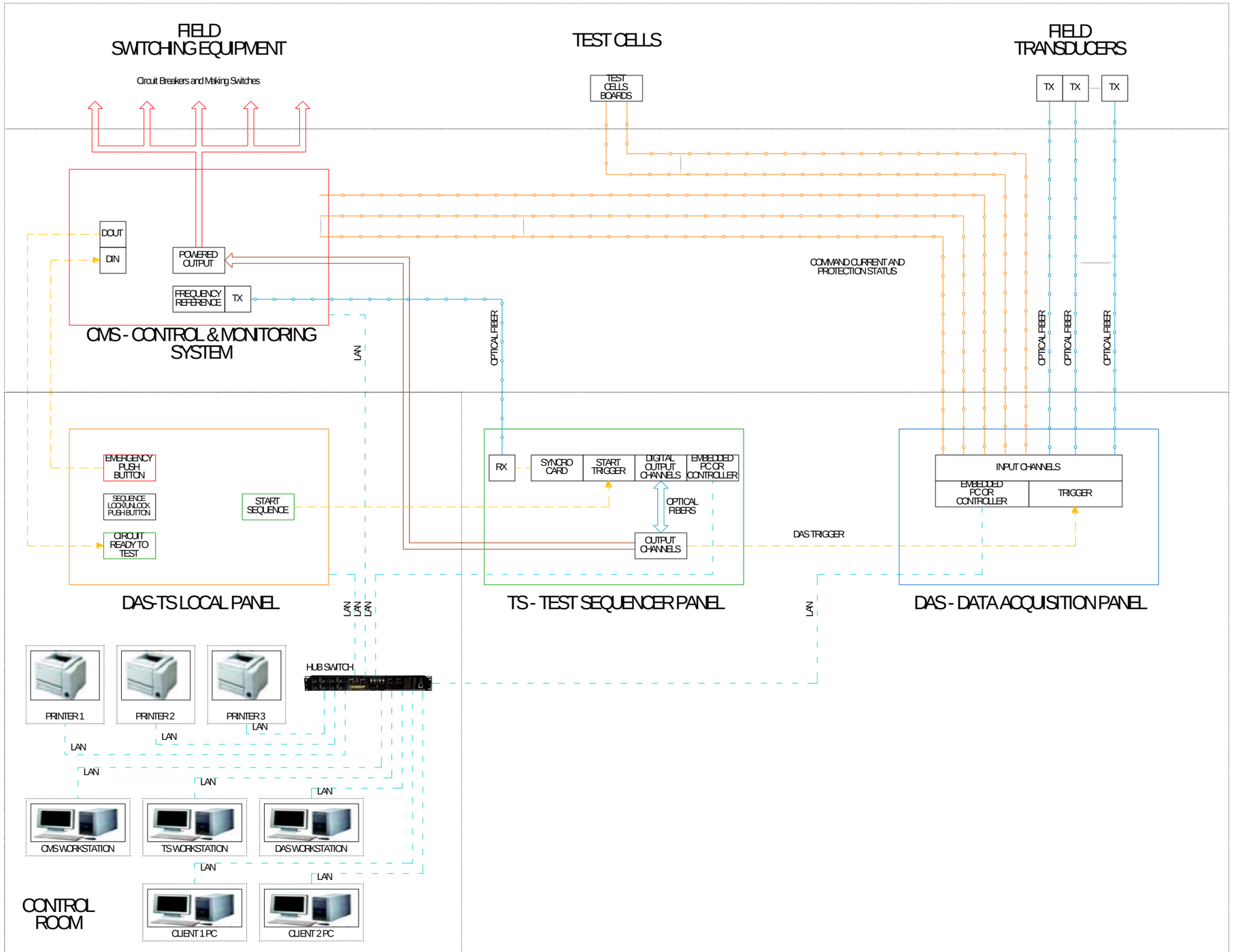
The supplier shall have to propose and quote for recommended spares with a minimum validity of one year. Recommended spares quote shall not be included in the main equipment cost for bid evaluation purpose. The supplier shall also guarantee for spares availability for the next ten years.

The supplier shall indicate the maintenance schedule proposed during the guarantee period and service life of the various items of equipment offered, when operated and maintained in accordance with instructions of the manufacturers.

11 WARRANTY

The equipment shall be guaranteed for 12 months from the date of installation and commissioning.

12.0 INTERCONNECTION DIAGRAM BETWEEN CMS-TS-DAS


FIELD SWITCHING EQUIPMENT
Circuit Breakers and Making Switches
TEST CELLS
TEST CELLS BOARDS
FIELD TRANSDUCERS
TX
TX
TX
DOUT
DIN
POWERED OUTPUT
FREQUENCY REFERENCE
TX
CMS - CONTROL & MONITORING SYSTEM
COMMAND CURRENT AND PROTECTION STATUS
LAN
OPTICAL FIBER
OPTICAL FIBER
OPTICAL FIBER
OPTICAL FIBER
EMERGENCY PUSH BUTTON
SEQUENCE LOCK/UNLOCK PUSH BUTTON
CIRCUIT READY TO TEST
START SEQUENCE
RX
SYNCRO CARD
START TRIGGER
DIGITAL OUTPUT CHANNELS
EMBEDDED PC OR CONTROLLER
OPTICAL FIBERS
OUTPUT CHANNELS
DAS TRIGGER
INPUT CHANNELS
EMBEDDED PC OR CONTROLLER
TRIGGER
DAS-TS LOCAL PANEL
TS - TEST SEQUENCER PANEL
DAS - DATA ACQUISITION PANEL
LAN
LAN
LAN
LAN
HUB SWITCH
PRINTER 1
PRINTER 2
PRINTER 3
LAN
LAN
LAN
LAN
LAN
LAN
LAN
LAN
CMS WORKSTATION
TS WORKSTATION
DAS WORKSTATION
LAN
LAN
CONTROL ROOM
CLIENT 1 PC
CLIENT 2 PC

13.0 PRELIMINARY LIST OF TEST SEQUENCER OUTPUT COMMANDS

The following tables provide examples of association of the Test Sequencer output channels to controlled equipment for the various test cells.

Control Room 1: HPTR Test Cell

TEST SEQUENCER OUTPUT COMMAND			
Channel No.	*Channel name*	*Description*	*Note*
1	Superexcitation_G1_ON	Generator G1	(1)
2	Superexcitation_G1_OFF	Generator G1	(1)
3	Superexcitation_G2_ON	Generator G2	(1)
4	Superexcitation_G2_OFF	Generator G2	(1)
5	Superexcitation_G3_ON	Generator G3	(1)
6	Superexcitation_G3_OFF	Generator G3	(1)
7	MB(17.5)1_ON	Master Circuit-breakers	(1)
8	MB(17.5)1_OFF	Master Circuit-breakers	(1)
9	MB(17.5)2_ON	Master Circuit-breakers	(1)
10	MB(17.5)2_OFF	Master Circuit-breakers	(1)
11	MB(17.5)3_ON	Master Circuit-breakers	(1)
12	MB(17.5)3_OFF	Master Circuit-breakers	(1)
13	MS(17.5)1_U_ON	Making Switch	(1)
14	MS(17.5)1_U_OFF	Making Switch	(1)
15	MS(17.5)1_V_ON	Making Switch	(1)
16	MS(17.5)1_V_OFF	Making Switch	(1)
17	MS(17.5)1_W_ON	Making Switch	(1)
18	MS(17.5)1_W_OFF	Making Switch	(1)
19	MS(17.5)2_U_ON	Making Switch	(1)
20	MS(17.5)2_U_OFF	Making Switch	(1)
21	MS(17.5)2_V_ON	Making Switch	(1)
22	MS(17.5)2_V_OFF	Making Switch	(1)
23	MS(17.5)2_W_ON	Making Switch	(1)
24	MS(17.5)2_W_OFF	Making Switch	(1)
25	MS(17.5)3_U_ON	Making Switch	(1)
26	MS(17.5)3_U_OFF	Making Switch	(1)
27	MS(17.5)3_V_ON	Making Switch	(1)
28	MS(17.5)3_V_OFF	Making Switch	(1)
29	MS(17.5)3_W_ON	Making Switch	(1)
30	MS(17.5)3_W_OFF	Making Switch	(1)
31	MS(17.5)R1_ON	Making Switch	(1)
32	MS(17.5)R1_OFF	Making Switch	(1)
33	MS(17.5)R2_ON	Making Switch	(1)
34	MS(17.5)R2_OFF	Making Switch	(1)
35	MS(17.5)R3_ON	Making Switch	(1)
36	MS(17.5)R3_OFF	Making Switch	(1)

TEST SEQUENCER OUTPUT COMMAND			
Channel No.	*Channel name*	*Description*	*Note*
37	MS(36)1_1_ON	Mobile Making Switch	(2)
38	MS(36)1_1_OFF	Mobile Making Switch	
39	MS(36)1_2_ON	Mobile Making Switch	
40	MS(36)1_2_OFF	Mobile Making Switch	
41	END_SEQUENCE	Sequence End to CMS	
42	DAS_TRIGGER	Trigger the Data Acquisition System	
43		SPARE	
44		SPARE	
45		SPARE	
46		SPARE	
47		SPARE	
48		SPARE	

Notes:

(1) CMS system shall dispatch these commands to the corresponding equipment of each of the short-circuit generators selected for the test.

(2) Gate signals are consents to be given before operation of controlled equipment to prevent operations (such as closing of a making switch) at incorrect timing. The presence and number of such control signals and relevant equipment shall be confirmed based on manufacturer's instruction.

Control Room 2: Test Cell 3.4 and New Test Cell 3.5

TEST SEQUENCER OUTPUT COMMAND			
Channel Nr.	*Channel name*	*Description*	*Note*
1	Superexcitation_G1_ON	Generator G1	(1)
2	Superexcitation_G1_OFF	Generator G1	(1)
3	Superexcitation_G2_ON	Generator G2	(1)
4	Superexcitation_G2_OFF	Generator G2	(1)
5	Superexcitation_G3_ON	Generator G3	(1)
6	Superexcitation_G3_OFF	Generator G3	(1)
7	MB(17.5)1_ON	Master Circuit-breakers	(1)
8	MB(17.5)1_OFF	Master Circuit-breakers	(1)
9	MB(17.5)2_ON	Master Circuit-breakers	(1)
10	MB(17.5)2_OFF	Master Circuit-breakers	(1)
11	MB(17.5)3_ON	Master Circuit-breakers	(1)
12	MB(17.5)3_OFF	Master Circuit-breakers	(1)
13	MS(17.5)1_U_ON	Making Switch	(1)
14	MS(17.5)1_U_OFF	Making Switch	(1)
15	MS(17.5)1_V_ON	Making Switch	(1)
16	MS(17.5)1_V_OFF	Making Switch	(1)
17	MS(17.5)1_W_ON	Making Switch	(1)
18	MS(17.5)1_W_OFF	Making Switch	(1)
19	MS(17.5)2_U_ON	Making Switch	(1)
20	MS(17.5)2_U_OFF	Making Switch	(1)
21	MS(17.5)2_V_ON	Making Switch	(1)
22	MS(17.5)2_V_OFF	Making Switch	(1)
23	MS(17.5)2_W_ON	Making Switch	(1)
24	MS(17.5)2_W_OFF	Making Switch	(1)
25	MS(17.5)3_U_ON	Making Switch	(1)
26	MS(17.5)3_U_OFF	Making Switch	(1)
27	MS(17.5)3_V_ON	Making Switch	(1)
28	MS(17.5)3_V_OFF	Making Switch	(1)
29	MS(17.5)3_W_ON	Making Switch	(1)
30	MS(17.5)3_W_OFF	Making Switch	(1)
31	MS(17.5)R1_ON	Making Switch	(1)
32	MS(17.5)R1_OFF	Making Switch	(1)
33	MS(17.5)R2_ON	Making Switch	(1)
34	MS(17.5)R2_OFF	Making Switch	(1)
35	MS(17.5)R3_ON	Making Switch	(1)
36	MS(17.5)R3_OFF	Making Switch	(1)
37	MS(36)1_1_ON	Mobile Making Switch New Test Cell 3.5	(2)
38	MS(36)1_1_OFF	Mobile Making Switch New Test Cell 3.5	
39	MS(36)1_2_ON	Mobile Making Switch New Test Cell 3.5	
40	MS(36)1_2_OFF	Mobile Making Switch New Test Cell 3.5	
41	TB_ON	Circuit-breaker under test Test Cell 3.4	
42	TB_OFF	Circuit-breaker under test	

TEST SEQUENCER OUTPUT COMMAND			
Channel Nr.	*Channel name*	*Description*	*Note*
		Test Cell 3.4	
43	END_SEQUENCE	Sequence End to CMS	
44	DAS_TRIGGER	Trigger the Data Acquisition System	
45		SPARE	
46		SPARE	
47		SPARE	
48		SPARE	

Notes:

(1) CMS system shall dispatch these commands to the corresponding equipment of each of the short-circuit generators selected for the test.

(2) Gate signals are consents to be given before operation of controlled equipment to prevent operations (such as closing of a making switch) at incorrect timing. The presence and number of such control signals and relevant equipment shall be confirmed based on manufacturer's instruction.